



## BEST AVAILABLE COPY

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3  
ular aspect of the present invention, a  
onic devices are disposed in a stack  
electronic device has an edge having  
a location thereon and wherein elec-  
arranged to expose the contact loca-  
edge by forming a stepped surface  
side of the electronic device stack.  
A particular aspect of the present in-  
onic device stack is disposed against a  
a plurality of contact locations  
ag at least one substrate contact loca-  
connected to at least one contact loca-

particular aspect of the present inven-  
tional interconnection between the chip  
and the substrate contact location  
local conductor bearing elastomeric  
posed between the chip contact loca-  
tation contact location.

A particular aspect of the present in-  
vonic device stack has at least one  
face for thermal connection to a heat

## BRIEF DESCRIPTION OF THE DRAWINGS

matic representation of one chip hav-  
ing thereon along an edge electrically  
substrate having contact locations  
the chip subtends a non-orthogonal  
to the substrate.  
A plurality of chips stacked in a non-  
alignment.

in elongated cylinder having electri-  
cally thereon which is used as the  
hector between the chip contact loca-  
tation contact locations in the embod-  
FIGS. 4 and 5.

A chip stack of FIG. 2 with the struc-  
ture electrical interconnection means  
disposed in connection with the chip

larged view of the electrical intercon-  
FIG. 4.

non-orthogonal stacking of chips along  
pendicular directions.

Diagrammatically shows an apparatus and  
using the stacked structure described

A stacked structure electrically con-  
tacts by an interconnection means  
ad conductors in an elastomer.

Another embodiment of the stepped  
present invention with contact location  
y connected to substrate contact loca-  
a.

BRIEF DESCRIPTION OF THE  
PREFERRED EMBODIMENT

view of an embodiment of the present  
FIG. 2 has at least one contact location 4  
to device 6 has at least one contact  
or surface 5 along an edge 10. Elec-  
as an opposite surface 7. Electronic  
an angle 12 with respect to substrate  
non-orthogonal angle, that is not 90  
device 6 contact location 8 is elec-  
to substrate contact location 4 by  
section means 13 which can be metal-

lized elastomeric body as described herein below, and  
which can also be a solder interconnection; wireboard  
array, patterned conductive epoxy; liquid metal; spring  
loaded or spring contacts; e.g., fuzx buttons or any  
other electrical interconnection means.

FIG. 2 shows a plurality of electronic devices 14, 16,  
18 and 20, which are stacked one on top of each other.  
Electronic devices 16, 18 and 20 are disposed in intimate  
contact with respect to each other. Electronic device 14  
is shown spaced away from electronic device 16 for the  
purpose of showing how the electronic devices are  
stacked. FIG. 2 shows four electronic devices in a stack.  
The structure of FIG. 2 is not limited to four, there can  
be any number of electronic devices in a stack. Each  
electronic device can be any type of an electronic de-  
vice such as a dielectric material having electrically  
conducting lines therein, for example a printed circuit  
board and a metallized ceramic. Alternatively, elec-  
tronic devices of FIG. 2 can be semiconductor chips,  
for example, silicon chips and gallium arsenide chips.  
Each electronic device is stacked onto an adjacent de-  
vice with an edge of each device set back by a distance  
22 from the adjacent device. The setback is preferably  
the same between each device. Each device has at least  
one contact location 24, preferably a plurality of  
contact locations along an edge region 26. The setback  
22 results in the contact locations 24 being exposed for  
each device. In the preferred embodiment, the top de-  
vice in the stack 14 is preferably a dummy device, that  
is having no electrical function but having a structural  
function but this is not necessary. If the setback 22 of  
each device is equal, the structure has a stack angle 28.  
The resultant stacked chip structure 30 has a stepped or  
staircased edge 32 with exposed electronic device  
contact locations and if the electronic devices are of the  
same dimension, there is a corresponding stepped or  
staircased surface 34 which can have additional chip  
contact locations or can be without device contact loca-  
tions. The structure of FIG. 2 shows each electronic  
device stepped back from an adjacent electronic device  
along the same direction 36. Between each adjacent  
electronic device such as 16 and 18 there is preferably  
an adhesive, such as an epoxy cement to keep each  
electronic device of the stack 30 physically adhering  
together. An adhesive layer is not shown in FIG. 2.  
Alternatively, the electronic devices of the stack 30 can  
be mechanically held together by a clamp. There may  
also be spacers placed between the devices.

FIG. 4 shows an electronic device stack 30 having  
nine electronic devices 40 in the stack. Electronic de-  
vice stack 30 edge 32 having the exposed electronic  
device contact locations is disposed adjacent surface 42  
of substrate 44. Surface 42 of substrate 44 has a plurality  
of contact locations 46 thereon. Contact locations 46 are  
electrically interconnected to contact locations 24 of  
electronic devices 40 by means 48 which can be a plu-  
rality of solder mounds disposed between electronic  
device contact locations 24 and a corresponding sub-  
strate contact location 46. Where solder mounds are  
used the controlled-collapse-chip-connection methods  
described in U.S. Pat. Nos. 3,401,126 and 3,429,640 to  
Miller, the teachings of which are incorporated herein  
by reference. Stepped edge 34 of electronic device stack  
30 which is opposite to stepped edge 32 is disposed in to  
a stepped groove 56 in the surface of heat sink 58. The  
stepped surface 34 of electronic device stack 30 pro-  
vides an enlarged surface area than would be provided  
if each electronic device were stacked orthogonally on

electronic device is located on the  
corresponding step 130 fixture 140 and not  
the previous electronic device.

(16) Step 5--Go to step two to load the  
next electronic device.

(17) FIG. 8 is a diagrammatical cross  
section, similar to that of FIG. 5,  
showing an alternate means for electrically  
interconnecting the electronic  
device contact pads 224 in electronic  
devices 240. Wires 250 are bonded at one  
end 252 thereof to the electronic device  
contact pads 224. The wires can be,  
for example, of Au, Al and Cu, for example  
of 0.001 to 0.003 inch diameter.  
The joint between ends 252 and contact  
locations 224 can be a wire bond. The  
bonds can be a flattened ball bonds or wedge  
bonds both of which are commonly  
practiced in the art. The wires are bent at  
an angle to the electronic devices  
surface 254 by jogging the bonder platform  
that the part rests upon after to  
bond is made. The end 256 of wire 250 is  
severed at a predetermined position.  
The ends 256 may be bent, laser-formed into  
ball shapes or left as straight  
wires. End positions may be manipulated to  
assure a given grid geometry for  
contact to substrate contact locations 246.  
The array is then encapsulated in  
an elastomeric, e.g. silicone, material  
leaving the ends of the leads free.  
There are two preferred methods for  
encapsulation of the leads. The first is  
to fixture the array so that the balls form  
a plane at the top of the part, and  
then to introduce a controlled volume of  
liquid encapsulant into the area of  
the leads. The spaces between the leads  
fills by capillary attraction and  
stops at the base of the balls. The liquid  
is then cured at elevated  
temperature. The second method is to first  
encase the lead ends in a water  
soluble solid, i.e., sugar, by dipping into  
the liquid form and then drying.  
Liquid elastomer is then forced under  
pressure into the space to be filled and  
cured. The water soluble cap is then  
dissolved away exposing the ends of the  
leads. The assembly may be pressed to the  
substrate or solder bonded as  
described above to the substrate contact  
locations 246 on substrate 244.

(18) FIG. 9 shows another embodiment of  
the stepped stack of chips shown in  
FIG. 2. The stack is disposed on a  
substrate 260 having a plurality of

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Sheet 1 of 8

5,239,447

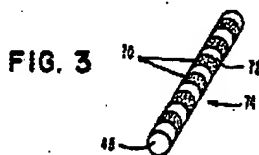
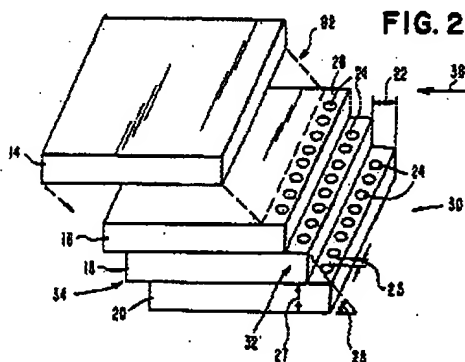
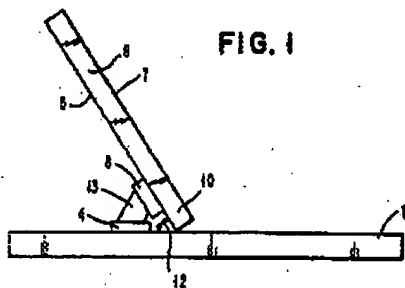


FIG. 1

FIG. 2

FIG. 3

In a more particular aspect of the present invention, a plurality of electronic devices are disposed in a stack and wherein each electronic device has an edge having at least one contact location thereon and wherein electronic devices are arranged to expose the contact location on each chip edge by forming a stepped surface along at least one side of the electronic device stack.

In another more particular aspect of the present invention, the electronic device stack is disposed against a substrate having a plurality of contact locations thereon, there being at least one substrate contact location electrically connected to at least one contact location.

Another more particular aspect of the present invention is the electrical interconnection between the chip contact location and the substrate contact location through an electrical conductor bearing elastomeric body which is disposed between the chip contact location and the substrate contact location.

In another more particular aspect of the present invention, the electronic device stack has at least one other stepped surface for thermal connection to a heat dissipation means.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic representation of one chip having contact locations thereon along an edge electrically connected to a substrate having contact locations thereon wherein the chip subtends a non-orthogonal angle with respect to the substrate.

FIG. 2 shows a plurality of chips stacked in a non-orthogonal arrangement.

FIG. 3 shows an elongated cylinder having electrically conducting bands thereon which is used as the electrical interconnector between the chip contact locations and the substrate contact locations in the embodiments shown in FIGS. 4 and 5.

FIG. 4 shows the chip stack of FIG. 2 with the structure of FIG. 3 as the electrical interconnection means and a heat sink disposed in connection with the chip stack.

FIG. 5 is an enlarged view of the electrical interconnection means of FIG. 4.

FIG. 6 shows non-orthogonal stacking of chips along two mutually perpendicular directions.

FIG. 7 diagrammatically shows an apparatus and method for fabricating the stacked structure described herein.

FIG. 8 shows a stacked structure electrically connected to a substrate by an interconnection means formed from formed conductors in an elastomer.

FIG. 9 shows another embodiment of the stepped structure of the present invention with contact locations thereon electrically connected to substrate contact locations by wire bonds.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a side view of an embodiment of the present invention. Substrate 2 has at least one contact location 4 thereon. Electronic device 6 has at least one contact location 8 on major surface 5 along an edge 10. Electronic device 6 has an opposite surface 7. Electronic device 6 subtends an angle 12 with respect to substrate 2. Angle 12 is a non-orthogonal angle, that is not 90 degrees. Electronic device 6 contact location 8 is electrically connected to substrate contact location 4 by electrical interconnection means 13 which can be metal-

lized elastomeric body as which can also be a solder array, patterned conductive loaded or spring contacts, other electrical interconnectors.

FIG. 2 shows a plurality 18 and 20, which are stacked. Electronic devices 16, 18 and 20 are shown spaced away from each other with respect to each other. FIG. 2 shows four devices stacked. The structure of FIG. 2 is shown in FIG. 3.

The structure of FIG. 2 is shown in FIG. 3. The structure of FIG. 2 is shown in FIG. 3. The structure of FIG. 2 is shown in FIG. 3.

FIG. 3 shows an elongated cylinder having electrically conducting bands thereon which is used as the electrical interconnector between the chip contact locations and the substrate contact locations in the embodiments shown in FIGS. 4 and 5.

FIG. 4 shows the chip stack of FIG. 2 with the structure of FIG. 3 as the electrical interconnection means and a heat sink disposed in connection with the chip stack.

FIG. 5 is an enlarged view of the electrical interconnection means of FIG. 4. FIG. 6 shows non-orthogonal stacking of chips along two mutually perpendicular directions.

FIG. 7 diagrammatically shows an apparatus and method for fabricating the stacked structure described herein. FIG. 8 shows a stacked structure electrically connected to a substrate by an interconnection means formed from formed conductors in an elastomer.

FIG. 9 shows another embodiment of the stepped structure of the present invention with contact locations thereon electrically connected to substrate contact locations by wire bonds.

FIG. 10 shows a stacked structure electrically connected to a substrate by an interconnection means formed from formed conductors in an elastomer.

FIG. 11 shows another embodiment of the stepped structure of the present invention with contact locations thereon electrically connected to substrate contact locations by wire bonds.

FIG. 12 shows a stacked structure electrically connected to a substrate by an interconnection means formed from formed conductors in an elastomer. FIG. 13 shows another embodiment of the stepped structure of the present invention with contact locations thereon electrically connected to substrate contact locations by wire bonds.